Improved Unsaturated to Saturated Logic Level Translation With Automatic Change on Reference Voltage

[1]Ganesh Adhikari, [2]Dr. Shashidhar Ram Joshi
[1]Associate Professor, [2]Professor
Electronics and Communication Department
Nepal College of Information Technology, Balkumari, Lalitpur, Kathmandu, Nepal.
Institute of Engineering, Pulchowk, Lalitpur, Kathmandu.
***Email:** ganeshadhikarireal@gmail.com, ganeshpa@nec.edu.np*

Abstract

This research relates to ECL to TTL converters for converting True ECL level signal to True TTL level signals and more particularly to converters which can operate at very fast switching speeds. It is an important achievement of this research work that resolves mixed voltage incompatibility between different parts of a system that operates in multiple voltage domains. They are common in today's complex systems, especially when interfacing with legacy devices with performance-optimized application specific level shifters for standard interfaces (e.g. SD card, SIM card). Another very important feature of the circuit is that the ECL reference voltage will automatically adjust by an appropriate percentage to compensate any shift slightly due to temperature change by utilizing the concept of voltage divider rule.

***Keywords:** TTL, ECL, VTC, Impedance*

INTRODUCTION

Level translator is an efficient solution for voltage matching. Circuit designers are faced with challenge of developing system with increasing functionality and complexity while under demanding power and time-to-market constraints. Such system often requires level translation devices to allow interfacing between integrated circuit devices built from different process technologies. It helps to find exact solution you need.

Translator phenomenon

Translator Phenomenon are common in today's complex systems, especially when interfacing with legacy devices. It offers the broadcast portfolio of standard, general purpose level shifters spanning a wide range of voltages, frequencies, bit widths and IO types (open drain or push-pull along with performance-optimized application specific level shifters for standard interfaces (e.g. SD card, SIM card).

Research Objectives

1. To provide 'Unsaturated ECL to Saturated TTL level translator' with improved switching speed.
2. To provide automatically adjusts ECL reference voltage level translator circuit with improved VTC for modified TTL gate.

Significance of study

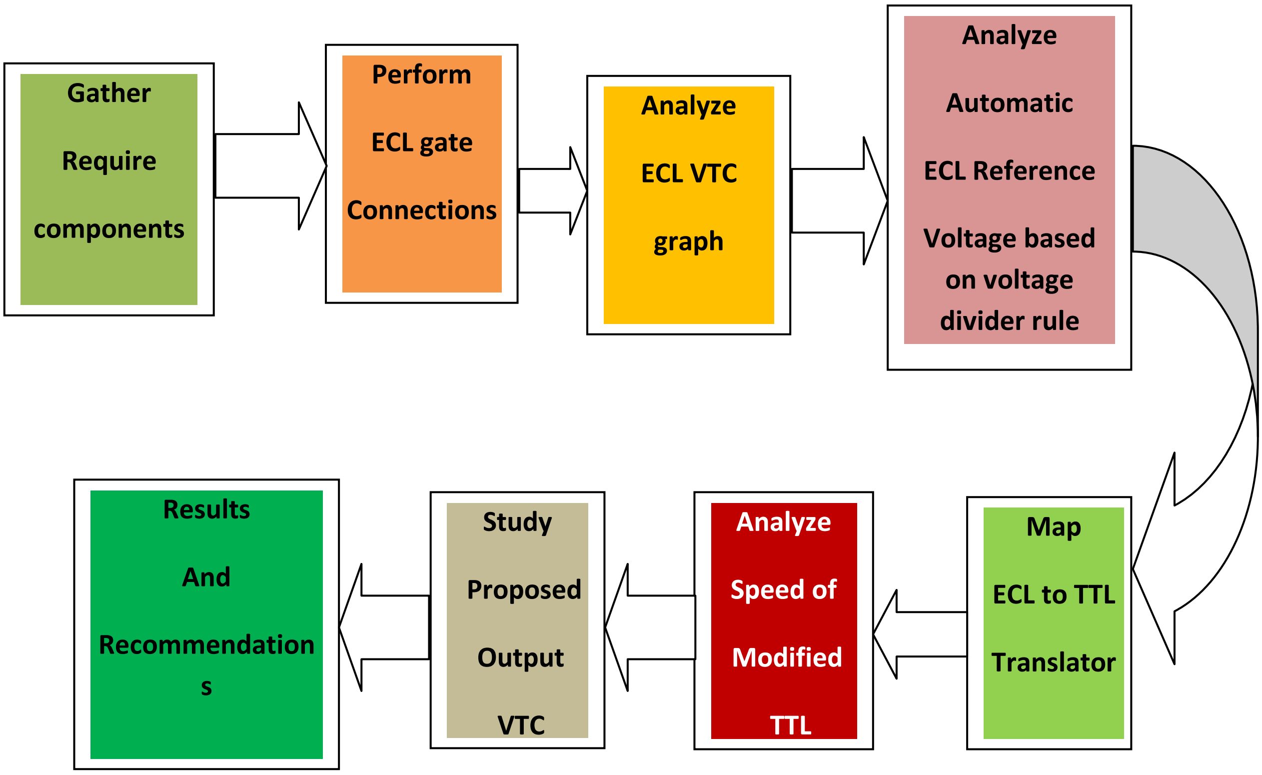
The unsaturated to saturated logic level translator is a group of combined circuit comprising of ECL gate, Temperature compensated ECL circuit and modified TTL gate.

The significance of study relates to unsaturated ECL to saturated TTL voltage level translator to increase switching speed by reduce propagation delay, increase fan-out, improved noise margin, low power consumption and automatic adjust in ECL reference voltage according to temperature change with improved VTC.

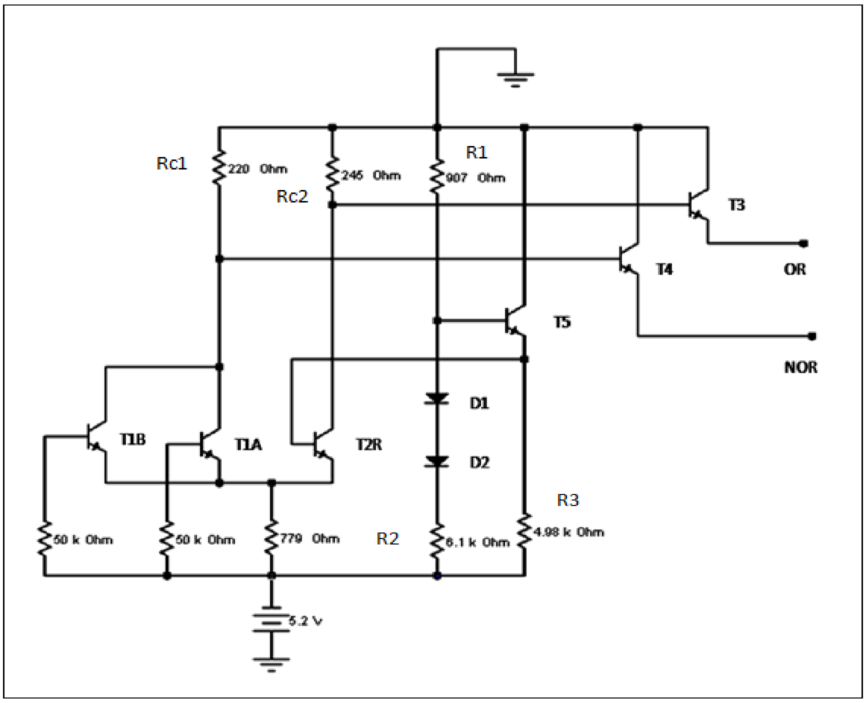
Today for very large scale integration of digital circuit, the level translator circuit becomes very important and useful especially when interfacing with legacy devices e.g. SD card, SIM card, Auto Codec, CF card, Gunning translation, IC-USB, SD/MMC card, UART etc.

RESEARCH METHODOLOGY

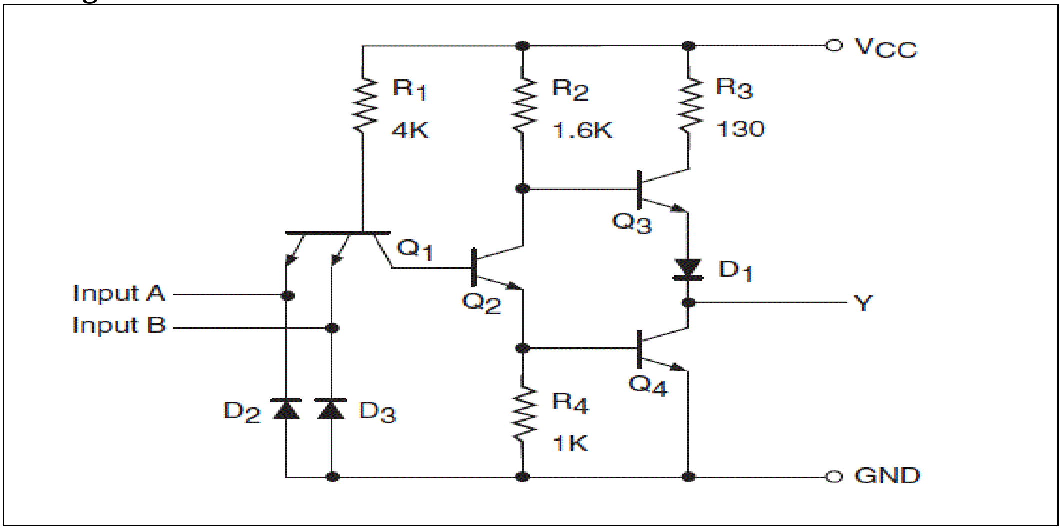
The purpose of research methodology is to provide a sound platform for the researcher to achieve the objectives of the study.



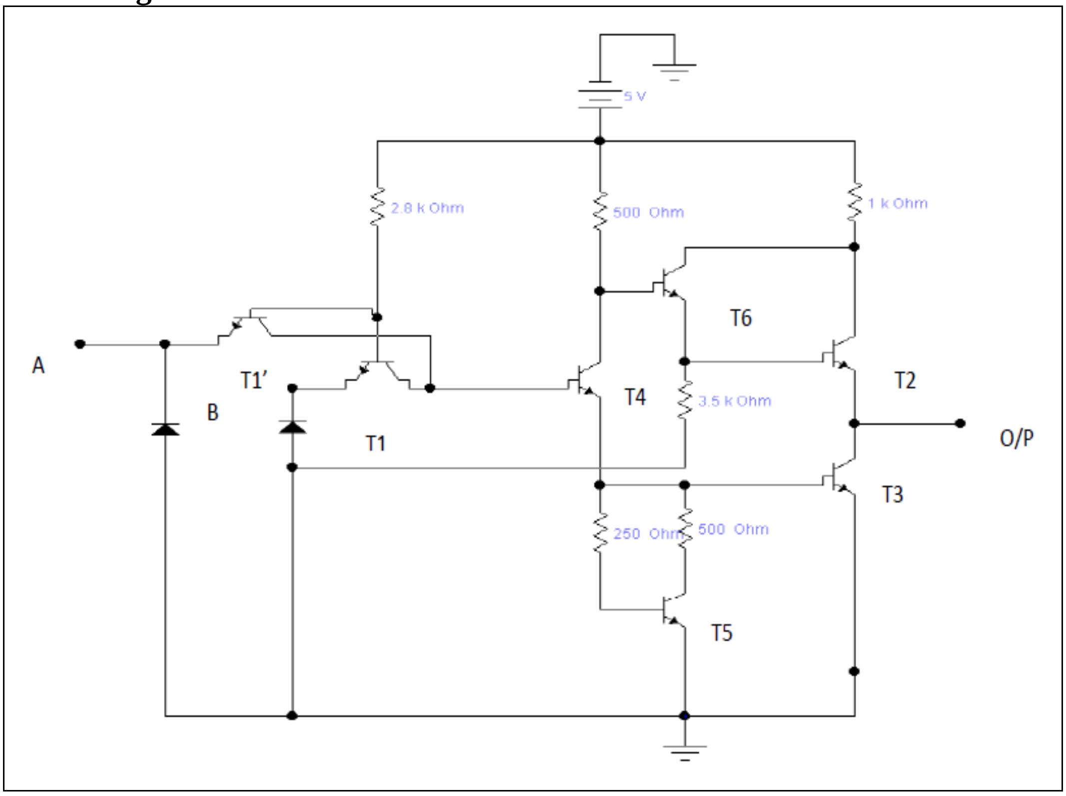
Basic ECLgate circuit



Basic TTL gate



Modified TTL gate



The TTL gate speed is further enhanced by proving modification on existing standard TTL gate, wherein fast charging is get accomplished through low output impedance emitter flower circuit i.e. transistor T2 followed by T6 and fast discharging is get accomplished via pull-down circuit transistor T5 followed by two resistors. This results in significant amount of reduction in propagation delay time there by increasing the switching speed of the circuit as very fast.

Comparison parameters (Gate behavior features of domains)

For comparative analysis, attributes of domain should be defined prior, which are the base of comparison.

- *Speed comparison of previous and modified TTL gate.*
- *VTC comparison of previous and modified TTL gate.*
- *Fan-out comparison of previous and modified TTL gate.*
- *Noise-margin comparison of previous and modified TTL gate.*

Study area

Transistor modeling

Computer Analysis

The appearance of a current controlled current source (CCCS) in the equivalent models of a transistor requires that the P-spice format for such a source be introduced. The format is introduced. The format is initialized by the letter F as shown below.

FBJT	3	2	VSENSE	0.98
Name	(+N)	(-N)	name of controlling Voltage source	magnitude of multiplier for Controlled source.

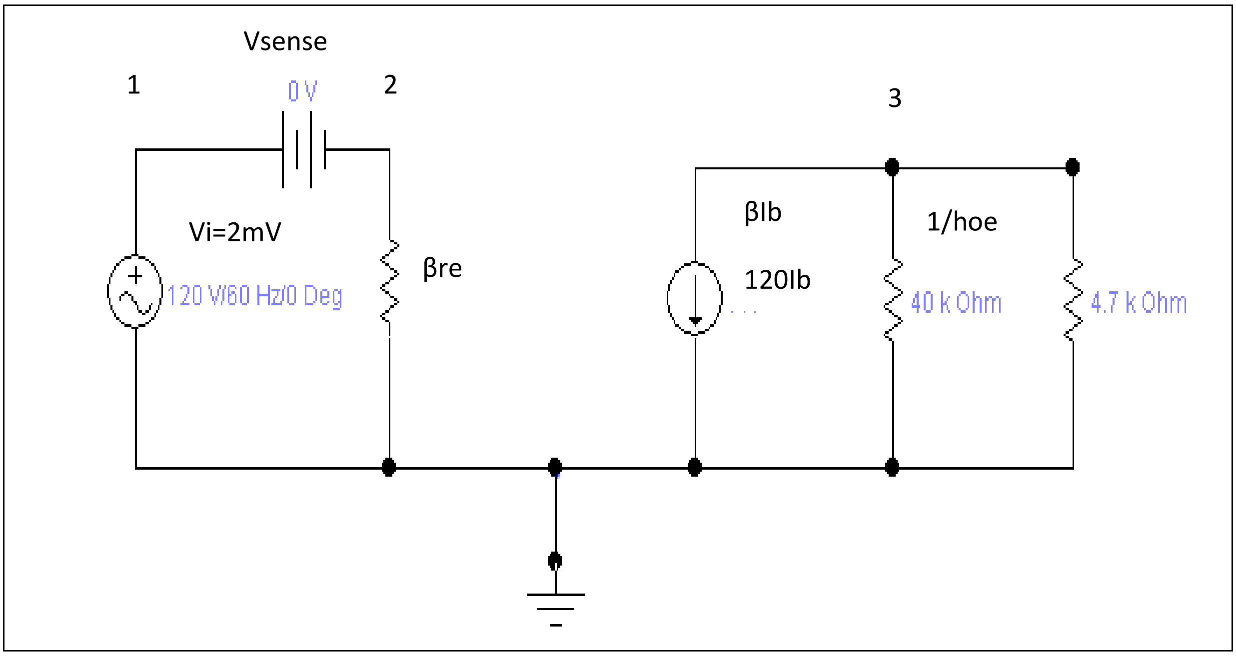


***Fig: 1** Common emitter amplifier*

P-spice analysis for CE network

```
Common-emitter amplifier
****     CIRCUIT DESCRIPTION
***************************************************************************************************************
VI  1  0  AC  2MV
VSENSE  1  2  0
RBRE  2  0  1.6K
FBETA  3  0  VSENSE  120
RO  3  0  40K
RC  3  0  4.7K
. AC  LIN  1  1K  1K
. PRINT  AC  VM(3,0)  VP(3,0)
. OPTIONS  NOPAGE
. END
**** SMALL  SIGNAL          BIAS  SOLUTION       TEMPERATURE  =  27.000  DEG  C
NODE      VLTAGE  NODE      VOLTAGE  NODE    VOLTAGE NODE     VOLTAGE
( 1) 0.0000       ( 2)0.0000        ( 3)  0.0000
VOLTAGE  SOURCE  CURRENTS
NAME                CURRENT
VI                  0.000E+00
VSENSE              0.000E+00
TOTAL  POWER  DISSIPATION           0.00E+00  WATTS
****     AC  ANALYSIS                                      TEMPERATURE  =  27.000  DEG  C
FREQ                VM(3,0)             VP(3,0)
 1.000E+03           6.309E-01           1.800E+02
```

Fig: 2 *P-spice analysis of the CE network*

Transfer function computation of 'Darlington Emitter Flower Circuit'

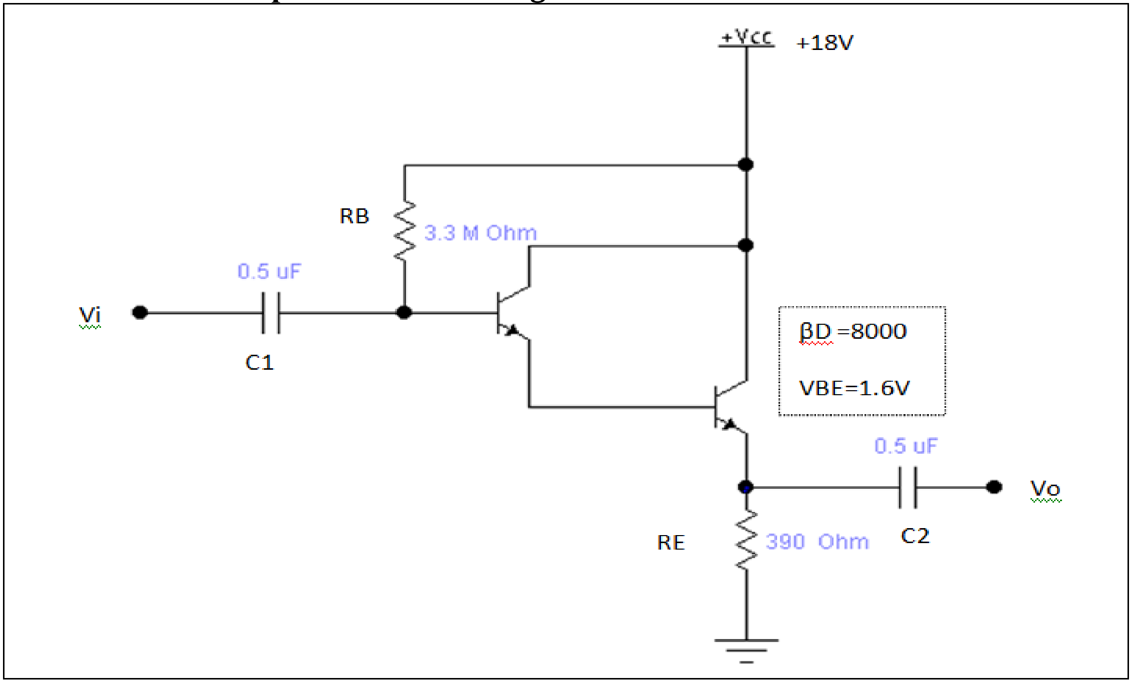


***Fig: 3** Darlington circuit parameters with specified values*

To compute input impedance

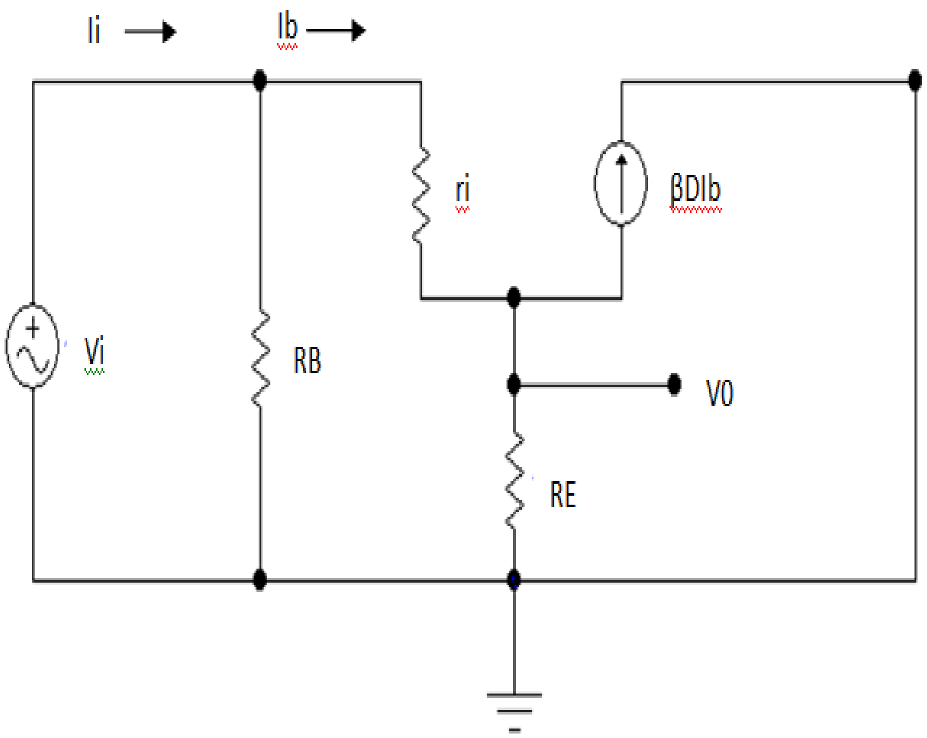


***Fig: 4** Hybrid circuit model for computing the input impedance of Darlington emitter flower Circuit.*

To compute output impedance

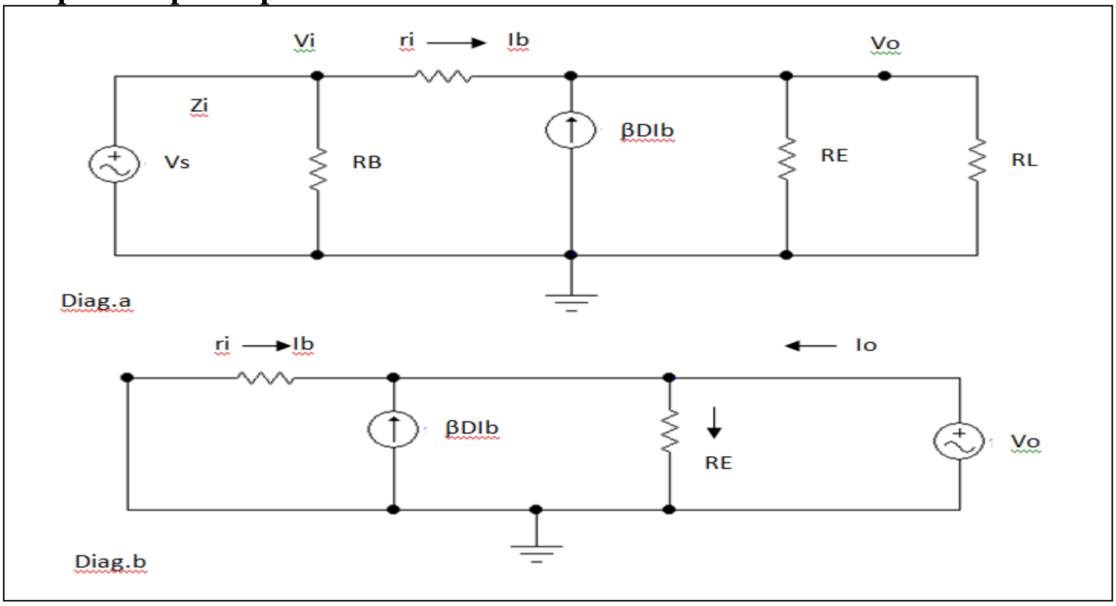


***Fig: 5** Hybrid circuit model for computing output impedance of Darlington Emitter flower circuits.*

To compute transfer function T(s)

The transfer function T(s), of a linear system with input impedance Zi and output impedance Zo is given by the expression

$T(s) = [Zo/Zi]$

$=[\{(R_E)||(ri)||(ri/\beta_D)\}/\{(R_B)||(ri+\beta_D R_E)\}]$

$=[(ri/\beta_D)/\{R_B||(ri+\beta_D R_E)\}]$

$=[(5K\Omega/8000)/\{(3.3M\Omega)||(5K\Omega+(8000)(390\Omega)\}]$

$=[(0.625\Omega)/(1.6M\Omega)]$

$T(s) \quad =0.39063*10^{-6}$

RESULTS AND DISCUSSION

This chapter deals with analysis of results obtained via different experiments. All the experiments are carried over various types of data sets related to selected scenarios.

Implementation details of standard TTL gate

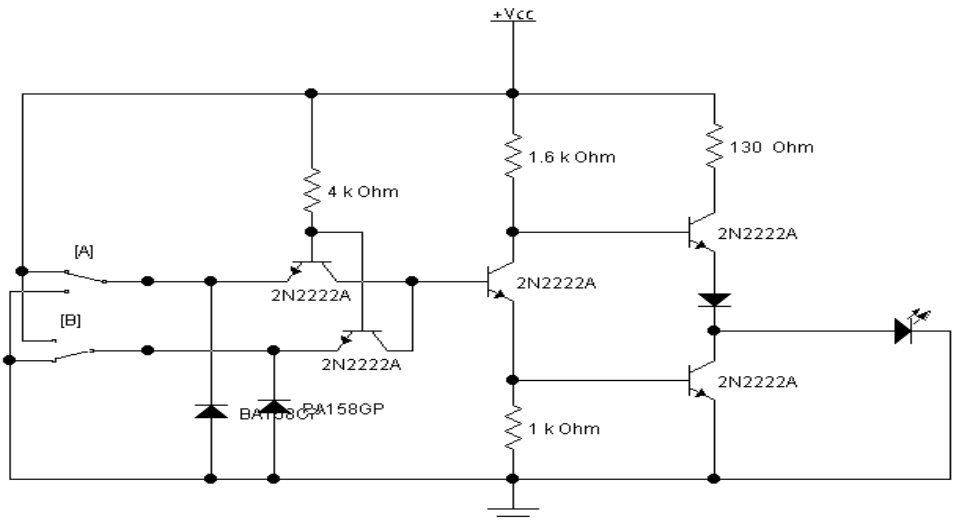


***Fig: 6** Workbench Simulation of Standard TTL Gate*

From above experiment parameter computed are as accordingly

V_{OH} = 741.6mV, V_{OL} = 8.4307mV, I_{OH} = 10 mA, I_{OL} = 4.8981mA.

V_{IH} = 5V, V_{IL} = 0.2V, I_{IH} = 0.01μA, I_{IL} = 0.05409μA.

Z_{OH} = 74.16MΩ.

Transition time from low to high (tp_{LH}) = 13 ns.

Transition time from high to low (tp_{HL}) = 8ns.

1. Noise-margin computation
2. High level noise margin = $|V_{OH} – V_{IH}|$ = |741.6mV – 5V| = 4.2584V.
3. Low level noise margin = $|V_{IL} – V_{OL}|$ =|0.2 V – 8.430mV|= 0.1915V.
4. Propagation delay
5. tp = [{tp_{LH} + tp_{HL}}/2] = [{13+8}/2] = 10.5ns.
6. Fan-out(N)

N = [I_{OH}/I_{IH}] = [10mA/0.01μA] = 1000*practically obtained [*Very high].

*Note: This value of fan-out is very high when computed from the actual data obtained from the experiment; but normally instead of "fan-out definition formula" N = [I_{OH}/I_{IH}], the analytically obtained formula (through analysis of TTL gate) N_H = [I_L/I_{IH}] is used to compute fan-out value.

N_H = [I_L / I_{IH}]

I_L = [{$V_{BE4(sat)}$ – $V_{CE4(sat)}$} / RC] = [{0.8 – 0.2} / 130**Ω**] = 4.6153mA.

I_{IH} = 0.06753mA.

N_H = [4.6153/0.0675] = 68.37 = 68 (approximately).

VTC of TTL gate

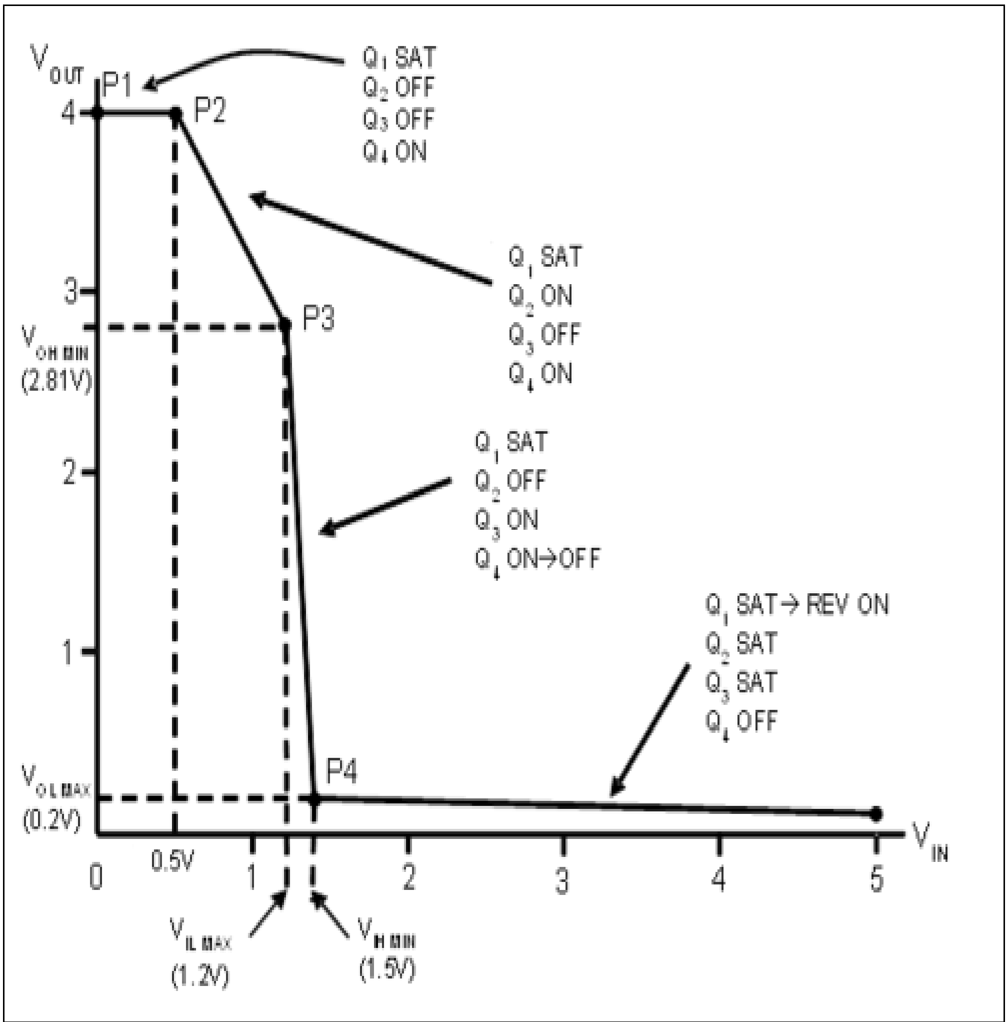


***Fig: 7** VTC of TTL gate*

Implementation details of modified TTL gate

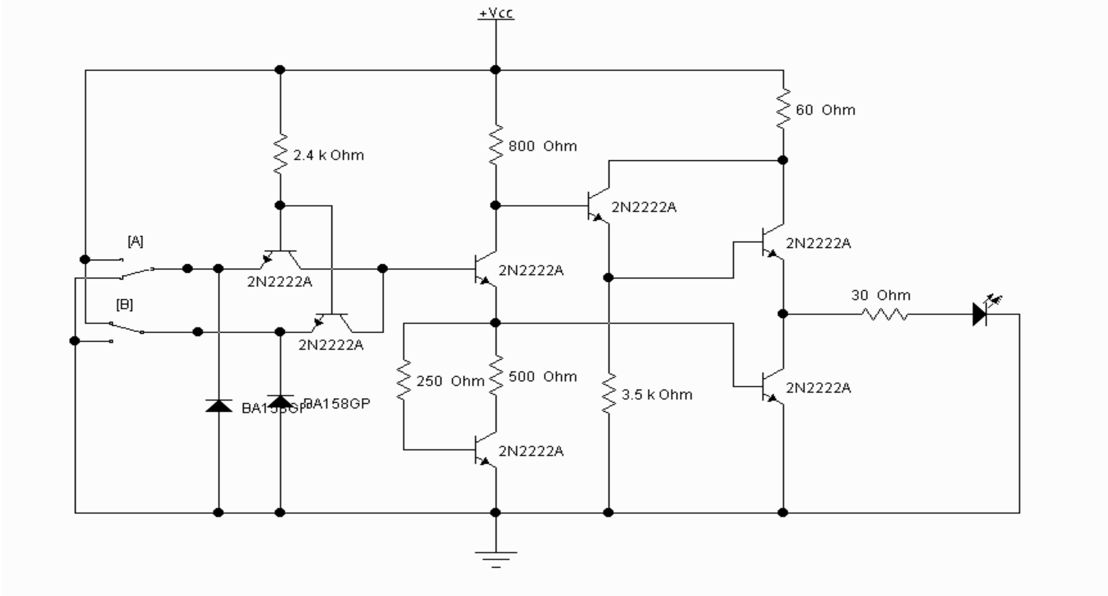


***Fig: 8** workbench simulation of modified TTL gate.*

From above experiment the parameters computed are as accordingly
V_{OH} = 750.2mV, V_{OL} = 10.23mV, I_{OH} = 10mA, I_{OL} = 327.7µA.
V_{IH} = 5V, V_{IL} = 0.2V, I_{IH} = 0.01µA, I_{IL} = 0.51705µA. Z_{OH} = 75.02MΩ

Propagation delay time from high to low = 9 ns.

1. Propagation delay time from low to high = 10 ns.
2. Propagation delay
   i. tp = [{tp_{LH}+tp_{HL}}/2] = [{9+10}/2] = 9.5ns.
3. Noise-margin computation
   a. High level noise margin = |V_{OH} – V_{IH}|= |750.2mV – 5V| = 4.2498V.
   b. Low level noise margin = |V_{IL} – V_{OL}| = |0.2V – 10.23mV|= 0.18977V
4. Fan-out[N]

N = [I_{OH}/I_{IH}]
= [10mA/0.01µA] = 1000*practically obtained [*Very high].
*Note: This value of fan-out is very high when computed from the actual data obtained from the experiment; but normally instead of “fan-out definition formula” N = [I_{OH}/I_{IH}], the analytically obtained formula (through analysis of modified TTL gate) N_H = [I_L/I_{IH}] is used to compute fan-out value.
N_H = [I_L / I_{IH}], From eq.[n] (3.9)
I_L = [{$V_{BE6\ (sat)}$ – $V_{CE6\ (sat)}$} / RC_2] = [{0.8 – 0.2} /60 Ω] = 10mA.
I_{IH} = 0.1125mA.
N_H = [10mA/0.1125mA] = 88.88 = 89 (approximately).

VTC of modified TTL

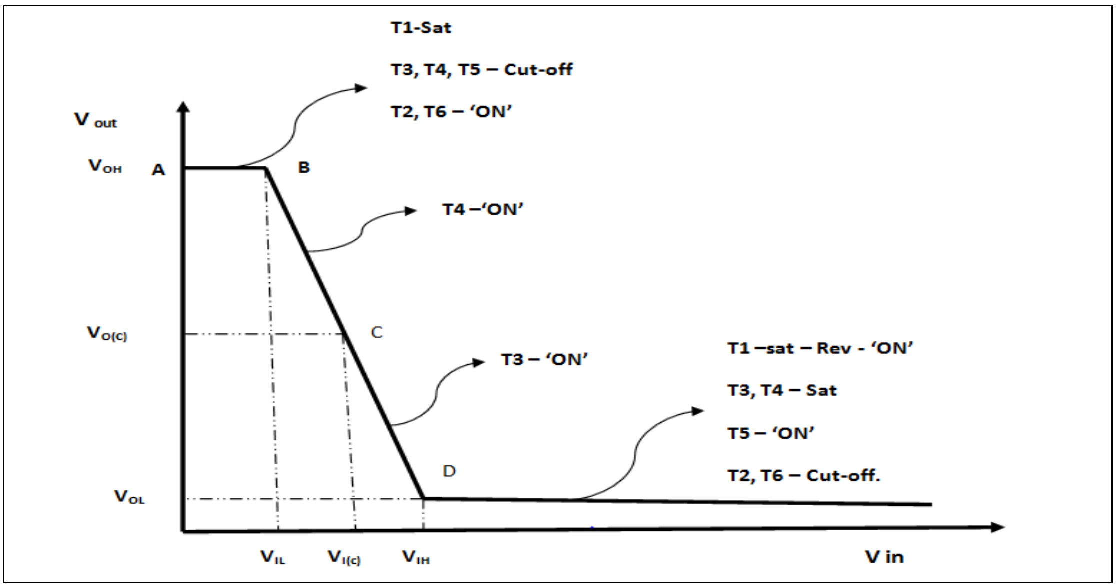


***Fig: 9** VTC of modified TTL gate*

Comparative analysis between TTL and Modified TTL gate

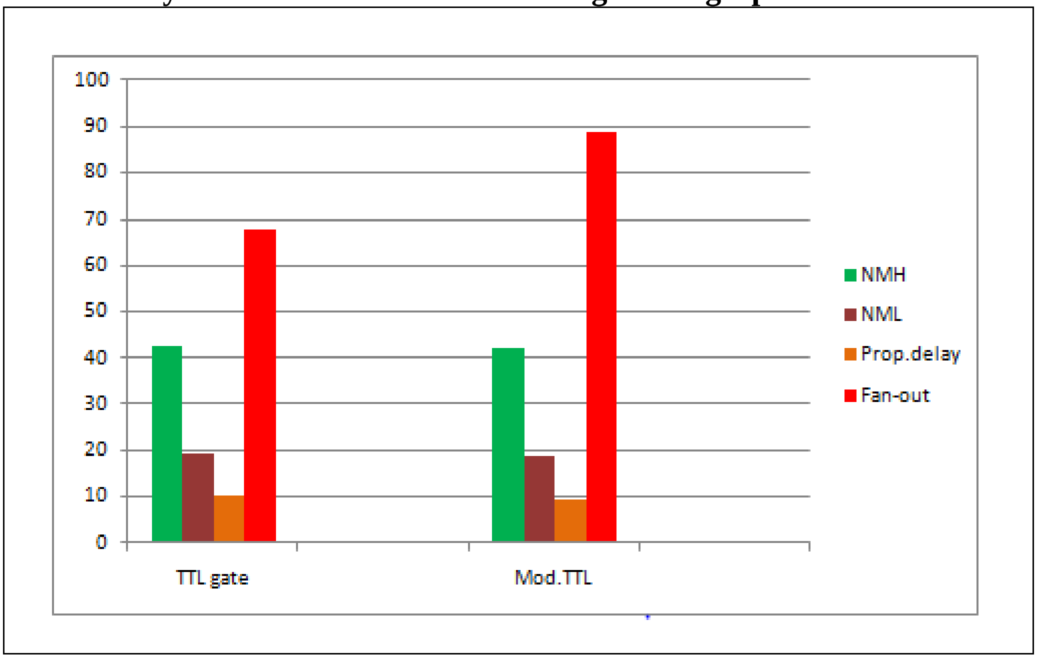
TTL gate

NM_H = 4.2584V
NM_L = 0.1915V
tp = 10.5ns
N = 68

Modified TTL gate

NM_H = 4.2498 V
NM_L = 0.18977V
tp = 9.5ns
N = 89

Comparative analysis of TTL and Modified TTL gate via graph

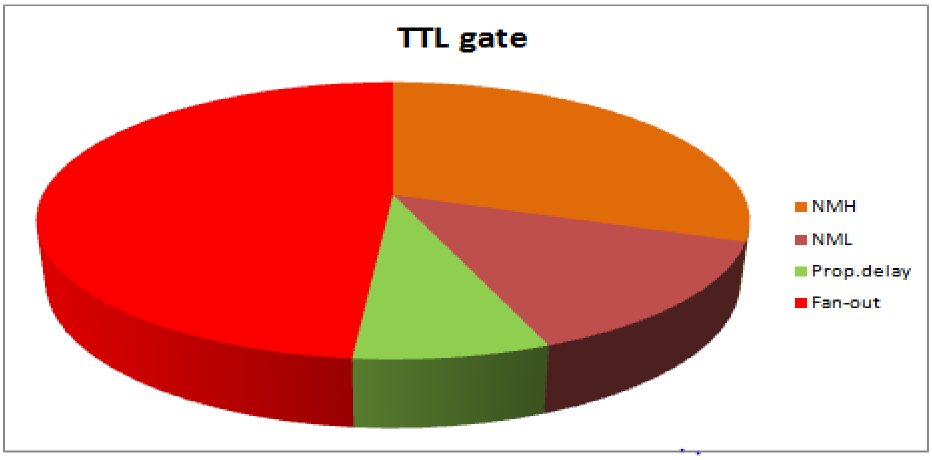


TTL gate

NM_H = 42.58V[M.F.= 10]
NM_L = 19.15V[M.F.= 1/10]
Prop.delay(tp) = 10.5ns[M.F.= 1]
Fan-out(N_H) = 68[M.F. =1]

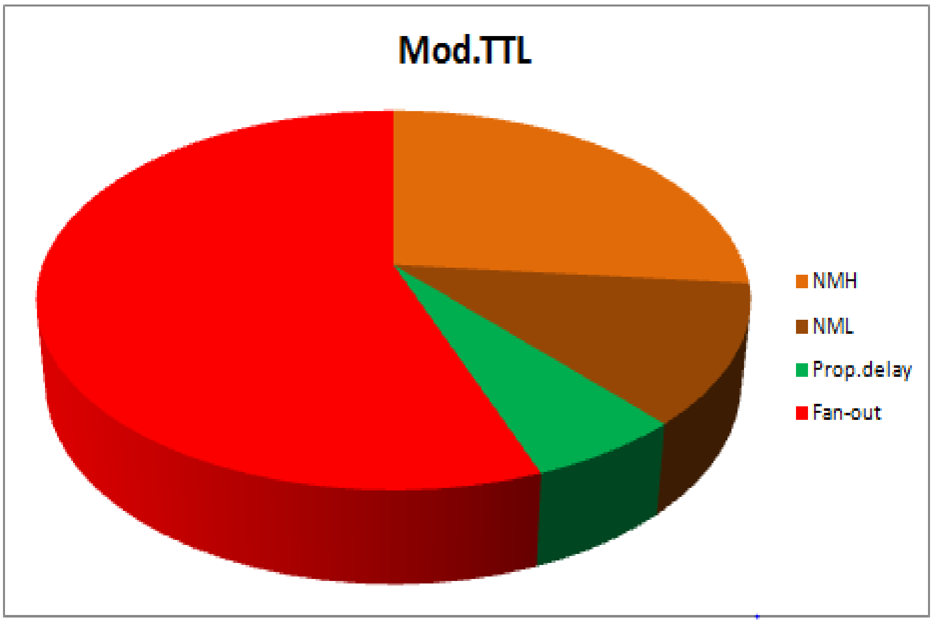
Modified TTL

NM_H = 42.49V[M.F.= 10]
NM_L = 18.97V[M.F.= 1/10]
Prop.delay(tp) = 9.5ns[M.F.= 1]
Fan-out(N_H) = 89[M.F. = 1]



NMH = 42.58V	NML = 19.15V	Prop.delay = 10.5ns	Fan-out = 68
[M.F.= 10]	[M.F. = 1/10]	[M.F. = 1]	[M.F. = 1]

Figure 4.8 Graph for TTL gate

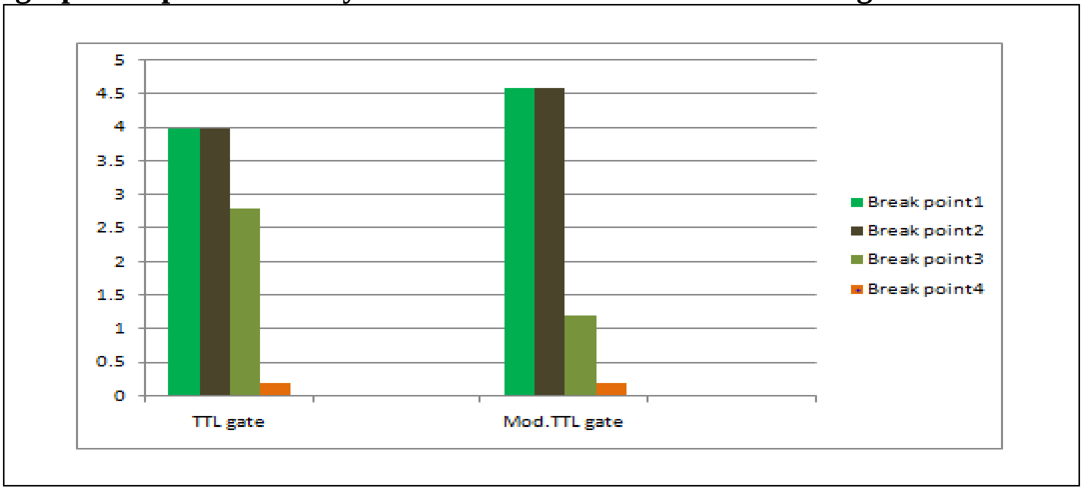


NMH = 42.49V	NML = 18.97V	Prop.delay = 9.5ns	Fan-out = 89
[M.F.= 10]	[M.F. = 1/10]	[M.F. = 1]	[M.F. = 1]

Figure 4.9 Graph for Mod. TTL gate

Fig 10. *Graph for Comparative analysis between TTL and Modified TTL*

VTC graph comparative analysis between TTL and Modified TTL gate



VTC Graph for comparative analysis between TTL and Modified TTL gate.

	Break point 1	Break point 2	Break point 3	Break point 4
TTL gate	4	4	2.81	0.2
Mod. TTL gate	4.6	4.6	1.2	0.2

CONCLUSION AND RECOMMENDATION

CONCLUSION

Fulfills both objectives mentioned on this research paper.

Switching speed of Modified TTL gate is faster than TTL gate switching speed.

VTC of Modified TTL gate results smooth operation than TTL gate [VTC] operation.

Limitations of study

Circuit ECL reference voltage becomes compatible only with Room temperature change.

Future Enhancement

- Enhance level translator circuit that becomes compatible even with higher variation of temperature change instead of room temperature change.
- Enhance level translator circuit with concept of “active emitter follower discharge path”
- Enhance a level translator circuit that could be mapped with Schottky TTL gate.

REFERENCES

1. Markks S Bimttella, Robert R, Walter C seelbach ‘ECL to TTL voltage level translator’ 17 Feb. 1987 and modified version published on 2013 on many papers - TTL activity – dmercer – approved version on 14-December 2012.
2. WIKIPEDIA, Overview for voltage level Translation, c, copyright 1995 – 2016 Texas instruments incorporated,file:///c:users/Lenevo/downloads/voltage
3. WIKIPEDIA, C, 2015, Oxford University Press, Reprinting or distribution, electronically or otherwise, without the express written consent of Oxford University press is prohibited.
4. Dario J Toncich 1994-Computer architecture, https://books.google.com.np/books)
5. WIKIPEDIA, electrical 4U.com, Transistor-Transistor Logic, c 2011 – 2017 electrical 4U, The content is copyrighted to electrical 4U and may

not be reproduced on other websites.
6. H.Taub and D.Schilling, Digital Integrated Electronics, Mc. Graw-Hill, New- York, New-edition, 2014.
7. Sedra and Smith “Microelectronic circuits” published by Oxford University Prwss.Inc. New York, Reprinted on 2012.
8. Robert L. Boylestad Louis Nashelsky “Electronic Device and Circuit Theory” Prentice-Hall, Inc. Englewood cliffs. N.J. U.S.A. 2008.
9. WIKIPEDIA, Activity: TTL inverter and NAND gate, This version (12-Dec.2013) approved by dmercer.
10. D.A. Hodges and H. G. Jackson, Analysis and design of Digital Integrated Circuit, Mc Graw – Hill, New edition 2013.
11. S. Singh, ‘High performance TTL Bipolar Integrated circuit in 4H – Sic’ Ph.D. dissertation, school of Elect. Comput. Engineering purdue University, West Lfayette IN 2015.
12. H.ELgabra, J.ELBoshra, N.ELsayed, M.Wahbah, S.Singh and M.ALZaabi, ‘High performance 4H – SiC, Emitter coupled logic circuit’ IEEE International conference on Electronics, Circuit and System, Abu Dhabi, UAE, December, 2013.
13. WIKIPEDIA, A technology for high temperature environments – IEEE paper on trans. Device, sept. 2012.
14. WIKIPEDIA, Bipolar integrated circuit in 4H SiC IEEE trans. Electron. Device –April 2011
15. L. Lanni, “Bipolar Integrated Circuits for High temp. application” – Ph.D – School Inform. Communic. Technology – Sweden 2012.
16. V.H. Grinich and H.G. Jackson, Introduction to Integrated circuits, Mc Graw-Hill, Latest edition, 2012.
17. J.E. Smith (ed.), Integrated Injection logic, IEEE Press, journal publication published Paper, New York, August, 2016.

BIBLIOGRAPHY

1. P.R. Gray and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 3nd ed; New York: Wiley, 1993.
2. G.W. Roberts and A.S. Sedra, SPICE, New York: Oxford University Press, 1992, 2nd ed; 1997.
3. A.S. Sedra and G.W. Roberts, ‘Current conveyor theory and practice,’ Chapter 3 in Analogue IC Design, London: Peter Peregrinus, 1990.
4. S. Soclof, Applications of Analog Integrated Circuits, Englewood Cliffs, N.J,:Prentice-Hall, 1985.
5. J.M. Steininger, ‘Understanding wideband BJT and MOS transistors,’ IEEE Circuits and Devices, vol. 6, no. 3 pp. 26 – 31, May 1990.
6. A.B. Grebene, Bipolar and MOS Analog Integrated Circuit Design, New York: Wiley, 1984.
7. L.E. Larson, K.W.Martin, and G.C. Temes, GaAs switched-capacitor circuit for high-speed signal processing, IEEE Journal of solid state circuits, December 1987.
8. P.R. Gray, D.A. Hodges, and R.W. Brodersen, Analog BJT and MOS Integrated Circuits, New York: IEEE Press, 2008.