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FPGA Implementation of Linear Frequency Modulation (LFM) Waveforms for Radar

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Abstract

The last few years have seen advances in radar signal generation and processing techniques with the development of powerful hardware and software. The key objective in designing a pulsed radar system is to attain a good range resolution and achieve maximum range detection. Pulse compression is a technique of signal processing that offers the advantages of greater range resolution capability as in case of short duration pulse and larger range detection capability of long duration pulse. Pulse compression using Linear Frequency Modulation (LFM) is a prevalent method in modern radar. In this proposed design, the LFM waveforms are generated using Direct Digital Synthesizer (DDS) technique. A carry save adder is used to optimize adder operations. The high speed adder architecture provides a greater system performance. This approach has been implemented on a Field Programmable Gate Array (FPGA) for the Radar application.

Keywords*: LFM, DDS, range resolution, pulse compression*

INTRODUCTION

The important aspects to be considered in generating radar waveforms are the ability to precisely produce and regulate the wave forms that give good resolving capabilities and attain larger detection range. Good resolution can be achieved with a shorter pulse. But conversely, shorter pulses need more peak power. The more tapered the pulse gets, its peak power must be increased such that enough energy is packed in the pulse.This increased peak power makes the design of transmitters and receivers more complex as the modules used to construct these need to tolerate the peak power. One method to overcome the problem is to transform the short pulse into a long one by means of some modulation technique to step up the bandwidth of the long pulse without compromising with the range resolution. This technique is known as Pulse Compression [1] and is used broadly in Radar applications where high peak power is adverse. Linear Frequency Modulation (LFM) is an important radar pulse compression technique as it achieves fewer side lobes, improved range resolution, achieve larger range and easily available in hardware. To design a radar signal transmitter, the physical parameters such as the magnitude, mass etc. of the system must be considerably lesser as possible. Generally, LFM signal generator is equipped with substantial weight and bulk components such as work station and other modules to generate the signal. On a contrary, the digital signal generator lacks large work station that reside in larger segment of the signal generator system[2]. In this paper, the generation of LFM signal and implementation is discussed. To begin with, the generation of LFM signal is

described, and then the LFM signal generation using DDS is explained.

Characteristics of LFM signal

Pulse compression: The mechanism of pulse compression is used in modern radar system signal processing wherein the tremendous energy of a stretched pulse width is combined with the great resolution of a smaller pulse width, thereby improving
detection capability [3]. Usually, the pulse is internally modulated in frequency or phase. Pulse compression radar transmits modulated long pulses and compresses the received echo signals into short pulses at the matched filter receiver.

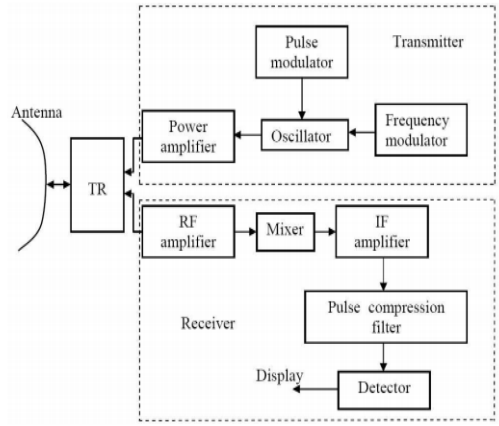

Fig. 1 Block Diagram of Basic Pulse Compression Radar

The pulse compression block diagram is as shown in the Figure (1). Here the pulse to be transmitted is modulated in frequency to increase the bandwidth. Trans-Receiver (TR) is the switching element to customize the same antenna as both transmitter as well as the receiver. The matched filter and its frequency response correlates with the transmitted waveform spectrum. The pulses obtained with comparable features to those of the pulses being transmitted are chosen by the matched filter while other signals are relatively passed over at the receiver.

Pulse radar system necessitates a high pulse power to achieve the preferred range. Concurrently, the transmission pulse width should be scaled down, since this limitation has an effect on the range resolution. These radars must be capable to produce and radiate the total emitted power in just a few micro or nano seconds.

Each part of the pulse has an individual unique frequency; the echo signal received can be entirely distributed in frequency and combined into a shorter width pulse at the output. The echo signal is therefore compressed in the pulse period in special filters. This operation is called pulse compression [4].

Definition of LFM signal:

The LFM signals are those in which the instantaneous frequency varies linearly in time across the pulse. The frequency may increase (up-chirp) or decrease (down-chirp) with respect to time.

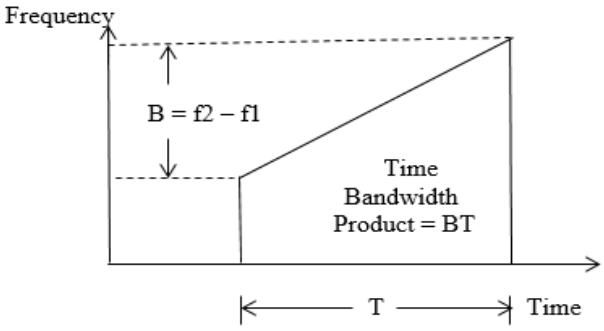

Fig. 2 Frequency of a Transmitted signal as a Function of Time

The Figure (2) shows that the frequency of the transmitted LFM pulse varies linearly in time across the pulse [5].

The phase of the chirp signal at an instant is expressed in the equation (1).

$$\phi(t) = 2\pi\left(f_0 t + \frac{1}{2}kt^2\right) \qquad (1)$$

where f_0 is the carrier frequency

k is the sweep rate of the frequency in correlation with the pulse duration T_p. The bandwidth B is specified as

$$k = B/Tp \quad (2)$$

The frequency at any time instant is linear as specified in the equation (3)

$$F(t) = d/dt\left(f_0t + \frac{1}{2}kt^2\right) = f_0 + kt \quad (3)$$

An ideal LFM waveform is represented in complex notation as

$$S_1(t) = Rect(t/\tau)exp(j2\pi(f_0t + (\mu/2)t^2)) \quad (4)$$

Where $Rect(t/\tau)$ represents the pulse width τ of a rectangular pulse.

Principle of DDS

DDS is a prevailing method that is being used to generate radio frequency signals in multiple applications from radio receivers to signal producers and various other applications. The DDS is a digital process of generating LFM waveforms for radar applications [6].

Digital Frequency Synthesizers

The term frequency synthesizer denotes an active electronic device as shown in Figure (3).

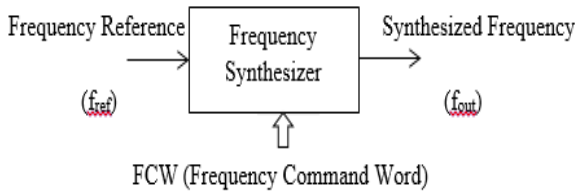

Fig. 3 Frequency Synthesizer

The block diagram of a frequency synthesizer is as shown in the figure (3). The synthesizer takes some frequency as reference (F_{ref}).This is an input signal of a constant frequency which produces frequency output such as instructed in the Frequency Command Word (FCW). The preferred output frequency values are obtained by FCW multiple of the reference frequency as per the equation

$$F_{out}=FCW.F_{ref} \quad (5)$$

LFM waveform generation using DDS

Direct Digital Synthesizer (DDS), which is a digital technique generates an analog waveform, commonly a sine wave by producing a time-variable signal in digital method and carrying out digital-to-analog transformation [7]. Since actions in the DDS system remain digital, they can deal with rapid switching frequencies, better resolution in frequency, also process over a wide-ranging band of frequencies.

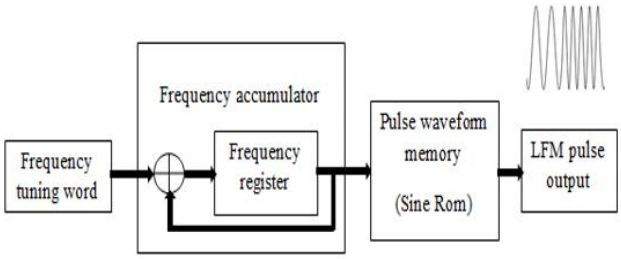

Fig. 4 Block Diagram to Generate LFM Signals using DDS

The Figure (4) shows block diagram to generate LFM waveforms using a DDS.

The DDS components mainly comprises of three core blocks – Numerically controlled Oscillator (NCO), sine ROM Look Up Table (LUT) and Digital-to-Analog Converter (DAC). The NCO consists of the phase accumulator and logic incremental register. This incremental register saves the binary values of frequency control register. The phase accumulator then adds phase addition value to its accumulator output. The output obtained from the accumulator calculated is being used to obtain the address in the sine LUT. This gives the digital binary values regarding the sine wave at the existing phase value.

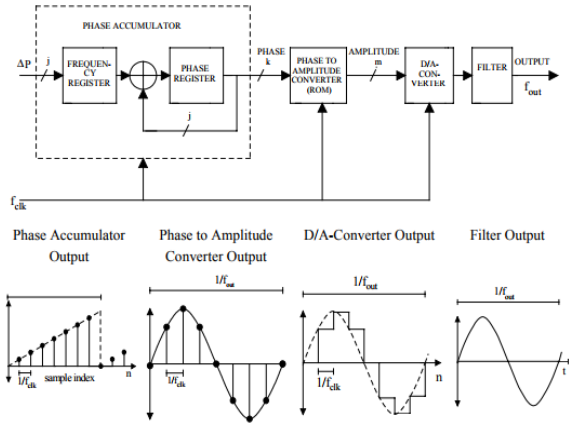

Fig. 5 Block Diagram of Basic Direct Digital Synthesizer and the Flow of signals in the DDS

A DDS functions by loading the points of the waveform in a digital format, then evoking them for generating the waveform. This rate by which the synthesizer finishes one complete waveform drives the frequency of the waveform [8]. The general block diagram is shown in the Figure (5).

The elementary function of the phase accumulator can be described more trivially in view of progression of the phase over the phase circle as shown in the figure (6).

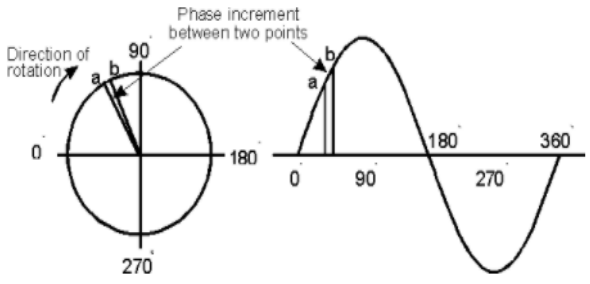

Fig. 6 Operation of a Phase Accumulator in DDS

The Figure (6) shows that, as the phase spreads all over the points of the circle, it matches to the progresses inside the waveform.

The frequency tuning word delivers the first input to the phase accumulator.

A sine LUT is used, in which the phase accumulator calculates an address for the corresponding phase (angle) in the LUT. Then a binary value of the amplitude is output analogous to that phase angle. These digital values are fed into the DAC, which consecutively transforms that resultant number to an equivalent voltage values in analog form.

Carry Save Adder (CSA)

Adders are a part of the elementary building units of every processor. In designing an adder, generating carry is the significant path towards decreasing the power dissipation in the data path in conjunction with the need to make the area of the adder smaller. The CSA is a very fast adder that is being used for many data path architectures.

Architecture of CSA

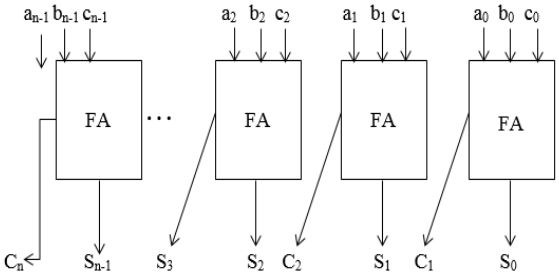

Fig. 7 n-bit Carry Save Adder

In a CSA, the carry is not circulated through the stages. As an alternative, carry exists in the current stage, furthermore provided as an add end number in the following stage. Therefore, the delay due to the carry is reduced in this structure [10].

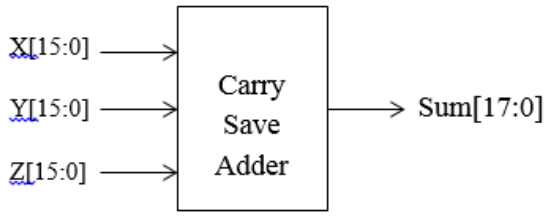

Fig. 8 Carry Save Adder Block

A CSA for 16 – bits input is described in the Figure (8). There are 3 inputs: X,Y and Z (16 bits each) and an output (18 bits). An example of carry save addition is shown below.

```
X:    10011          X:    10011
Y:  + 11001          Y:  + 11001
Z:  + 01011          Z:  + 01011
-----------          -----------
SC:   11011          PS:   00001
```

```
X:    10011
Y:  + 11001
Z:  + 01011
-----------
PS:   00001
      /////
SC:   11011
-----------
Sum:  110111
```

X + Y + Z = Sum + Carry

The carry save element comprises of n full adders, where each one calculates a single bit sum and carry. A set of 3 n-bit numbers X, Y and Z are considered. The adder performs addition and provides the results in as Partial Sum *PS* and a Shift-Carry *SC*.

The final sum is then retrieved by performing the following steps:

- Shift the array of carry *SC* left by 1 bit
- Adjoin a *0*to the MSB of *PS*
- At the final stage, these two results are added and produce the *Sum* as a result.

Simulation results

The DDS unit generates LFM pulse with the cited pulse width, sweep bandwidth, sweep interval and other parameters. The LFM waveforms are implemented using Verilog as a hardware description language. The phase accumulator,sine ROM as well as the CSA are all coded as 16-bits.

The proposed project realized on FPGA makes at ease to alter the parameters of the waveforms to suit the design at desired situations. Using FPGA to implement a DDS system would provide a moderate amount of design flexibility, since FPGAs can easily be reprogrammed and thus different solutions could easily be tested and compared to one another.

The simulation results of DDS are shown in Figure (9).

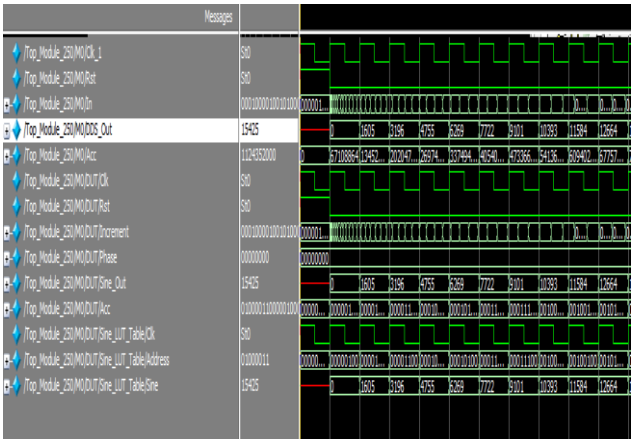

Fig. 9 DDS Simulation Output

The DDS is incorporated with a reference clock, a phase accumulator and control register, all 16-bits. The phase is incremented in the phase accumulator at regular clock intervals. On every clock tick, the adder adds the value of the phase increment word with the output of the adder. The adder outputs results obtained in the previous clock pulse due to the feedback connection. The Figure (10) shows simulation results of sine LUT.

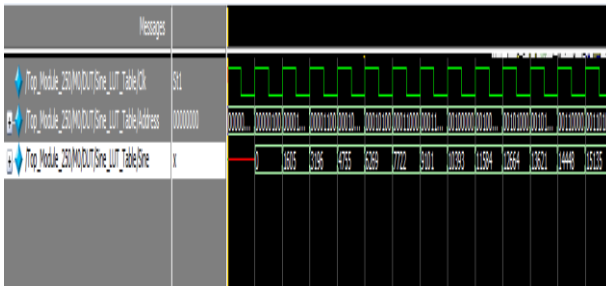

Fig. 10 Sine LUT Simulated Result

The sine LUT obtains phase increment values as the frequency tuning word. The DDS is driven by primarily saving samples of the waveform in binary form. These samples are then invoked pertaining to produce the waveform. From this, we can infer that there is predictable difference within one certain frequency and the following frequencies.

The plot of simulated LFM waveforms is shown in the Figure (10)

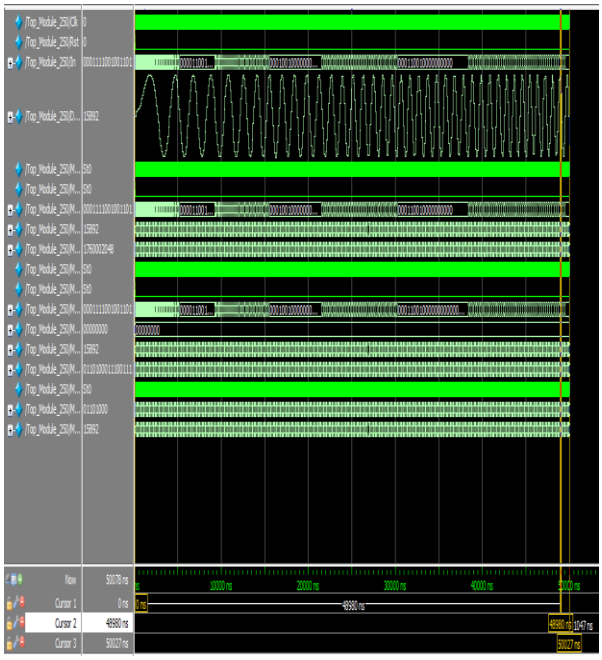

Fig. 10 Simulated Output of the Generated LFM Waveform

The Figure (10) shows that the frequency of the generated LFM waveforms is a linear function of time. The instantaneous phase varies constantly with time.

Table-1: Development specification of DDS Signal Generator

System requirements	Specifications
Band width	1 MHz
Pulse width	50 us
Reference clock	10 MHz
Length of phase Accumulator	16 bits
Sweep rate	4 KHz/0.2us

The LFM signal generator design specifications are presented in the table (1).

Bandwidth of the signal is set to 1 MHz. the frequency increases from 0-1 MHz in a pulse duration of 50us with a sweep rate of 4KHz/0.2us.This means that the phase of the phase of the LFM waveform varies 250 times within the pulse width of 50us. Carry Save Adder (CSA) is being used in this work as it is a more efficient technique to reduce the delay, area and power dissipation in implementing the LFM waveforms on FPGA. The table (2) shows the comparison of various adders implemented on FPGA.

Table-2: Comparison of Adders

Adders Method	Area of LUTs			Delay		
	LUT	Gate Count	Slices	Delay	Gate/ Logic Delay	Path/Route delay
BEC adder	78	66169	41	9.572 ns	4.400 ns 46.0%	5.172 ns 54.0%
Carry Select Adder	74	66148	41	8.75 ns	4.209 ns 48.1%	4.542 ns 51.9%
Ripple Carry Adder	72	66130	40	8.933 ns	3.779 ns 42.3%	5.154 ns 57.7%
Carry Save Adder	**35**	**65949**	**18**	**4.414 ns**	**2.126 ns 48.2%**	**2.288 ns 51.8%**

The comparison proves that the CSA is more resourceful and a high speed adder.

Improvement in the adder circuit speed, explicitly improves speed of the system. Here, we can arrive at an inference that the CSA which is employed in the project yields a considerable amount of reduction

in area and delay. Thus saving power significantly.

Conclusions

LFM, an intrapulse modulation technique is widely used in radar transmitters as it offers fewer side lobes, improved resolution, greater detection ranges and other advantages. The waveform generator was designed using a DDS structure considering various waveform parameters such as frequency bandwidth, pulse duration, sampling rate and other factors.

The key benefit of using DDS system in generating the LFM waveforms is that it can precisely manipulate the phase under digital processor control. The designed circuit generated LFM waveforms for radar pulse compression and was implemented on FPGA. In this work, a high speed adder architecture, CSA was employed to obtain a better optimization of the FPGA circuit with lesser delay and area consumption.

Scope and Future work

LFM waveforms are an excellent choice for pulse compression as they are programmable to achieve determinable ranges and suppress the noise. The LFM waveforms are generated using digital approach with DDS which gives the superior performance than analog methods.

Recent growths in digital signal generation are facilitating a higher degree of integration, more cost- and space- efficient waveform generators. In addition to extensive frequency coverage, sources for LFM generation must have rapid frequency and amplitude switching speeds to simulate different radars functioning in different modes at various frequency bands.

REFERENCES

[1] H A Said, A.A El-Kouney, A,E ElHenaway, "Design and realization of an efficient VLIC architecture for a linear frequency modulation (LFM) pulse compression in pulsed radars using FPGA", *AAFRICON, IEEE trans, ISBN:978-1-4673-5943-6, ISBN:ISSN:2153-0033,* 2013

[2] H Yang, S.B Ryu, H.C Lee, S.G Lee, S.S Yong, J.H Kim, "Implementation of DDS chirp signal generator on FPGA", *Information and Communication Technology Convergence (ICTC), IEEE conference, ISBN:978-1-4799-6786-5, DOI:10.1109/ICTC* 2014

[3] F Ning, W Yuze, X Hongwei, Q Liyan, J Hong, "Method of lfm pulse compression implementation based on FPGA", *Electronic Measurement & Instruments (ICEMI), IEEE conference, ISBN:978-1-4799-0759-5 DOI:10.1109/ICEMI* 2013

[4] S Ejaz, M.A Shafiq, Dr. M.J Mughal, "real time implementation of digital lfm pulse compression technique over acoustic waveguide", *International journal of Engineering and Technology Vol:10 No.4, pp. 22-25*

[5] T.T Mor, Su Su Yi Mon, "Pulse compression method for radar signal processing". IJSEA, Volume 3Issue 2, ISSN-2319-7560, pp. 31-35, 2014

[6] R.I Wijaya, S.N Ros, E.S Bagus, M Dadan, "FPGA based – Q chirp generator using first quadrant DDS compression for pulse compression radar", *AIP conference proceedings, Vol 1755, Issue 1, 170005,* 2016

[7] S S Desai, Prof. A.S Josh, "DDS architecture for digital frequency

generation*", IJARCET, Vol 2, Issue 1, pp. 107-111*, 2013

[8] G Guptha, M Kapoor, "an improved analog waveforms generation techniques using direct digital synthesizer", *International journal of Computer Applications (0975-8887) Vol 78- No.5*, 2013

[9] M Hortiz, J Hormingo, F Quiles, F.J Jaime, J Villalba, E.L Zapalta, "Efficient implementation of carry save adders in FPGA", *IEEE conference on application specific systems, Architectures and Processors*, 2009

[10] N U Azim, W Jun, "FPGA based hardware optimized implementation of signal processing system for LFM pulsed radar", *Proceedings of the SPIE, Vol 10030*, 2016