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# Design of EDDR Architecture Based on Approximate Arithmetic Adders

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***Abstract***

*This paper presents the design and simulation of design of EDDR architecture based on approximate arithmetic adders. Dynamic reconfigurable approximate arithmetic units are used to generate and get the original data. The motion estimation (ME) plays a significant role in a video coder, testing such a module is of main concern. Whereas focusing on the testing of ME in a video coding system this work presents an EDDR (error detection and data recovery) has been designed for excessive performance in software program implementation. To stumble on errors within the processing factors (PE) based totally on residue and quotient(RQ)code and for this reason, improves detection and facts recovery via the use of the proposed EDDR design for video coding testing application effectively. The design of the gadget is implemented and the language used to put in writing the code is Verilog after which is simulated using Modelsim6.4a. The software device used is Xilinx ISE design match 14.7.*

***Keywords:*** *Error detection and data recovery (EDDR), motion estimation(ME),processing elements(PE),residue and quotient(RQ)code.*

## INTRODUCTION

The progress in semiconductors, virtual sign processing, and communique technologies like multimedia packages more reliable and bendy. MPEG, JPEG superior Video Coding is the good example, which is widely appeared as the subsequent generation video compression general[1],[2] it is maximum necessary for massive sort of programs to lower the whole records amount is critical for transmitting or storing video records..In conjunction with the coding structures, an ME is of priority subject in exploiting the sequential redundancy among consecutive frames[4],[5], however, the maximum time ingesting issue of coding. In addition, whereas performing the computation encountered in the whole coding system, a ME is generally regarded as the majority computationally rigorous of a video coding system[3].

### *Reconfigurable Adder/Subtractor Blocks*

Dynamic variation of the DA can be carried out when each ofthe adder/subtractor blocks is prepared with one or more of its approximate copies and it could transfer among them as per requirement.

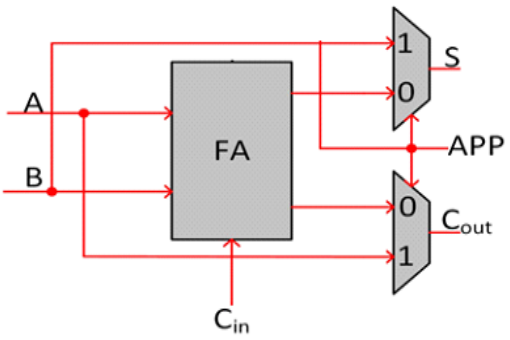


***Fig1.1****bit Dual mode full adder*

This reconfigurable architecture be capable of comprise in several approximate version of the adders/subtractors [6],[7] .Though in addition wants to be ensure with the purpose of the additional area overheads essential for constructing the reconfigurable approximate circuits are

minimal with sufficiently large power savings as shown in the above fig1.1 for example we have selected the two most known methods presented in ,specifically, truncation and approximation , for approximating the adder/subtractor blocks. The ultimate one can be conceptualized as an enhanced edition of truncation as it without delay relays the two 1-bit inputs, one as sum and the other as Carry Out (Choice 2), for the given inputs A, *B* and $C_{in}$ are the1-bit inputs to the full adder (FA), and the outputs are Sum=*B* and *Cout=A* .Therefore proving to be a improved approximation mode than truncation. The proposed method replace each FA cell of the adders/subtractors with a dual-mode FA (DMFA) cell (Fig. 2) in which each FA cell can activate either in entirely accurate or in a few approximation mode depending on the state of the control signal APP. A logic high value of the APP signal denotes that the DMFA is operating in the approximate mode.

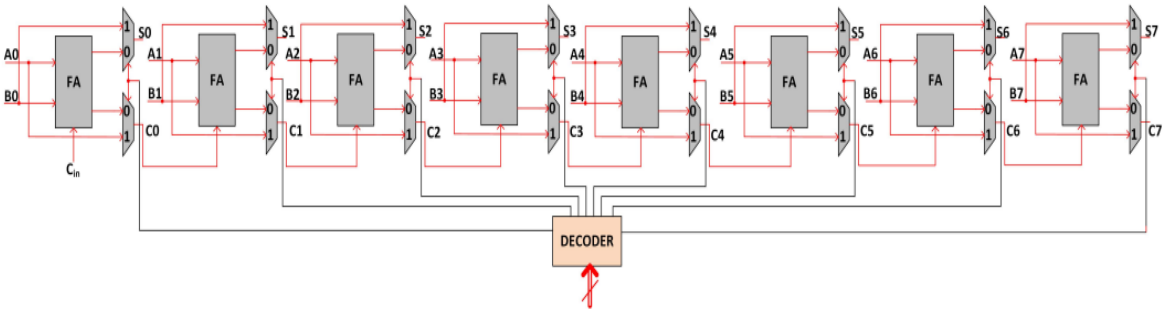


***Fig.2 8** bit reconfigurable RCA*

We term these adders/subtractors as ripple carry adders. It is significant to note that the FA cell is power-gated when working in the approximate mode. Assessment and synthesis of power utilization of a 16-bit RCA were performed in Synopsys. Power Compiler and its plan are the subsequent results are described in this experiments have shown a minor variation in the power utilization of DMFA when operated in either of the two approximation modes. Therefore, there is no loss of generalization; approximation was preferred for its high possibility of getting the correct output result than truncation, which consistently outputs 0 irrespective of the input.Fig.2. Shows the logic block diagram of the DMFA cell, which replaces the essential FA cells of an 8-bit RCA, in adding together, it also consists of the approximation controller for generating the proper select signals for the multiplexers.

**PROPOSED EDDR ARCHITECTURE DESIGN**

The proposed EDDR scheme is shown in the fig4, which comprise two main circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to find the errors and to recover the consequent data in a precise The test code generator (TCG) in Fig.4. utilize the concepts of RQ code to produce the matching test codes for error detection and data recovery.

In further terms, the primary output and the test codes from TCG are delivered to EDC to verify whether errors are present or not. DRC is in charge of recovering of data from TCG.

In addition of these, a selector is enabling to send the recovered data or error free data. prominently, an array-based computing arrangement, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is possible for the proposed EDDR scheme to detect errors and recover the corresponding data .This work adopts the

systolic ME for testability to demonstrate the feasibility of the proposed EDDR architecture.

A ME consists of many PEs included in a 1-D or 2-D array for video encoding applications. A PE generally have 8 or 12 bit adders with accumulator(ACC) and 8-b ADD (a pixel has 8-b data) is used to calculate approximately the addition of the current pixel (Cur_pixel) and reference pixel (Ref_pixel). In order to that ACC and 12-b ADD are necessary to accumulate the results from the 8-bit ADD in order to find the sum of absolute difference (SAD) value for video in the equation (1) and the pixel values of 4*4 bits are Fig3 it consist of (Cur pixel and Ref_pixel).

| | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 0 | 128 | 128 | 64 | 255 |
| 1 | 128 | 64 | 255 | 64 |
| 2 | 64 | 255 | 64 | 128 |
| 3 | 255 | 64 | 128 | 128 |

Cur_pixel

| | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 0 | 1 | 1 | 2 | 3 |
| 1 | 1 | 2 | 3 | 4 |
| 2 | 2 | 3 | 4 | 5 |
| 3 | 3 | 4 | 5 | 5 |

Ref_pixel

***Fig3.*** *Example for pixel values*

$$\mathrm{SAD} = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} |X_{ij} - Y_{ij}|$$
$$= \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} |(q_{xij}\cdot m + r_{xij}) - (q_{yij}\cdot m + r_{yij})| \quad \ldots\ldots\ldots(1$$

***Fig 4.*** *Proposed EDDR Architecture*

### *B.TCG Design*

In order to Fig.4, TCG is a significant module of the proposed EDDR architecture. particularly, TCG design is based on the capability of the RQCG circuit to produce equivalent test codes in order to detect errors and recover data. The Fig.3 estimates the absolute difference between the Cur_pixel and the Ref_pixel of the corresponding RCQG code so TCG circuit design easily achieve

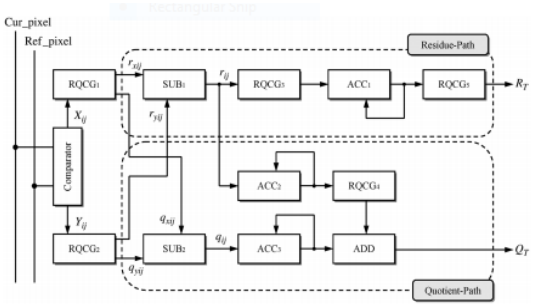


***Fig5.*** *TCG*

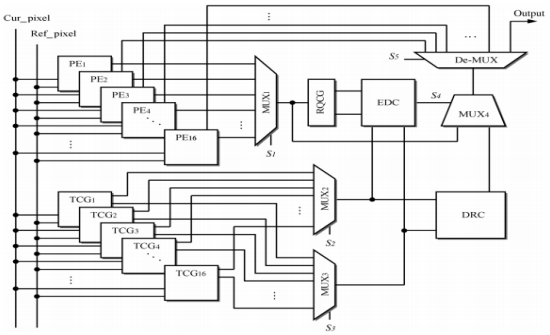


***Fig 6.*** *Proposed EDDR architecture for ME*

The above Fig6 indicates that the operations of error detection in a specific is achieved by using PE's,EDC,RQCG, DRC and with DMFA which is utilized to compare the outputs between TCG and in order to find whether the errors have been occurred. If the values of and/or, then the errors in particular can be detected. The output of the EDC is then used to generate a 0/1 signal to indicate that the tested is error-free.

## SIMULATION RESULTS

All the units in the process were designed. These units were written in VHDL modules and it is synthesized using Xilinx ISE Design suit 12.4 and Models simulator is used to verify the functionality of each block. RTL view for of proposed EDDR generated from Xilinx ISE is shown in Fig7.

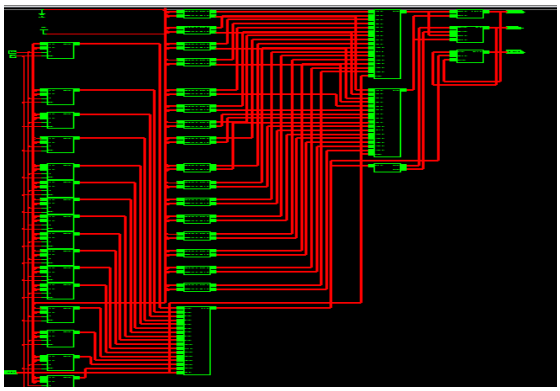

***FIG7.*** *RTL VIEW*

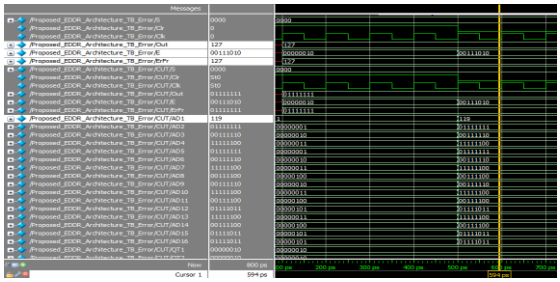

***FIG 8.****WITH ERROR*

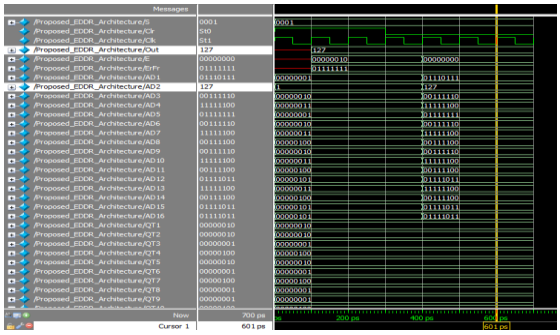

***FIG 8.*** *WITHOUT ERROR*

## CONCLUSION

We have simulated a EDDR architecture with proposed motion estimation successfully for calculating error and detecting with approximate mode VHDL language on ModelSim simulator. This lets that SAD algorithm is one of the powerful tool method for calculation of pixel in videos like JPEG, MPEGetc. by using simple dual mode adders /subtractors. And also by using RCA no of clock cycle can be reduced, performance increases, LUT size can be reduced and major multiplication and division block eliminated.

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