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Design and Implementation of Phase Locked Loop for Distributed Generation Systems

Ansilen.D[1],Gogulraja.S[2],Gopinath.B[3],Jackson Noel Francis.C[4]
FINAL YEAR EEE, SARANATHAN COLLEGE OF ENGINEERING, TRICHY
[1]Email Id:ansilendon@gmail.com
[2]Email Id:gogulraja22@gmail.com
[3]Email Id:gopispecial3@gmail.com
[4]Email Id:jackson.nf.007@gmail.com

Abstract

This project work concentrates on design and implementation of grid frequency synchronization of three phase inverter fed grid connected system. Initially, three phase inverter with sinusoidal PWM technique has been simulated with MATLAB/Simulink for RL load. As a next step, the design of LC filter has been carried out to generate sinusoidal waveform because the grid is subjected to disturbance as modulating wave frequency modifications, it is obligatory to preserve the frequency of grid linked to strength gadget at 50 Hz. The Grid frequency synchronization alongside amplitude and phase perspective of grid, via segment locked loop method has been supplied. The entire setup is implemented in real time by generating sine PWM pulses with the help of Arduino ATmega328P microcontroller.

Keywords: *Grid connected system, LC filter, Inverter.*

INTRODUCTION

Phase Locked Loop(PLL)which turned into particularly used for synchronous reception of radio signals. After that, PLL strategies were broadly used in various industrial fields which includes induction heating energy substances, contactless power materials, communication structures and motor manage structures. in recent times, PLL strategies had been used for synchronization among grid-interfaced converters and the application network[1]. a really perfect PLL can offer the quick and correct synchronization information with a excessive diploma of insensitivity and immunity disturbances, harmonics unbalances, sags or swells, notches and different styles of distortions in the enter sign. This paper ambitions at providing a comprehensive survey on various PLL synchronization strategies to facilitate the proper choice for precise packages. Phenomena like harmonics, frequency variations and voltage unbalance often arise in the application grid. Any PLL working primarily based on grid voltage or modern-day measurements should be designed so that you can segment lock quickly and convey a low distortion output below all conceivable grid situations.

DESIGN OF LC FILTER

Inverters are utilized in dispensed generator in everyday lifestyles. The primary problem is injection of harmonics in grid device. Those harmonics require the connection of Low pass filters between the inverter and the community. The passive clear out now not most effective have an effect on inverter harmonic injection however impacts on the harmonics produced with the aid of a coupled non-linear load [2]. Passive clear out technique used in this project is LC clear out.

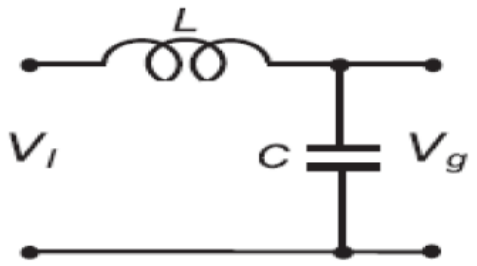

Fig1

LC–Filter — Second order

The LC-clear out in figure 1 consists of a shunt detail which is needed to reduce the switching frequency additives. This shunt issue should be decided on to produce low reactance on the switching frequency. But a few point of control frequency range, this detail need to present a high magnitude impedance. The primary shunt element used on this venture is Capacitor. The resonant frequency is calculated from equation 2.1.

$F=1/(2\pi\sqrt{LC})$ (2.1)

The LC-filter in Figure 1 has been investigated in UPS systems with an impedance across C is relatively high in the LC filter which is shown in figure 1 and above the switching frequency in this method. The reactive power consumption of the LC-filter is high than any other filter because of the addition of the shunt element.

Most low order harmonics are attenuated in LC low pass filter out in the output voltage waveform. The inverter output impedance has to be minimized to reduce the distortion in linear or non-linear loads. Consequently the capacitance price must be maximized and the inductance cost ought to be minimized whilst specifying the cut-off frequency This reduces the total cost, weight, volume and $Q((\sqrt{L}\sqrt{C})/R)$. But the inverter power rating will be increased by increasing the capacitance due to this process reactive power increase. Based upon Switching frequency in high power application is chosen inverter efficiency, since switching losses are a major portion of the overall losses. It is taken in account to minimize the size and cost of the filtering components by increasing the switching frequency, but efficiency sets a limit.

The low frequency harmonic components are reduced by the inductor which indicates the inductor current ripple. The phase voltage of The SPWM inverter phase voltage in the proposed system is shown in Figure 2.

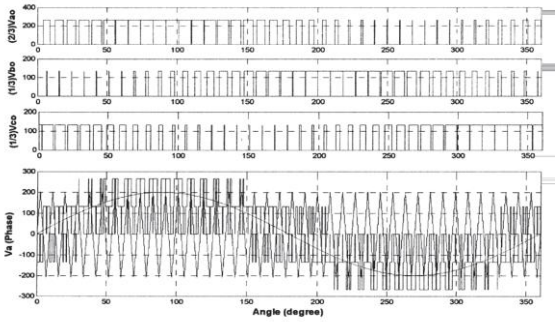

Fig2

V_a is the inverter phase voltage in Figure 2, and assume that the output voltage V_{ga} and its slowly varies relatively to the switching frequency. Then the across the inductor is:

$$V_L=V_{Ia}-V_{ga} \quad (2.2)$$

Via and *Vga* determines the maximum inductor ripple current as in equations (2.3) and (2.4). The phase voltage duty cycle at maximum output is 75%:

$$V_{Ia}=\frac{2}{3}V_{DC}, V_{ga}=\frac{1}{2}V_{DC} \quad (2.3)$$

$$V_L=(\frac{2}{3}V_{DC})-(\frac{1}{2}V_{DC})=\frac{1}{6}V_{DC} \quad (2.4)$$

The rated current is allowable to 10-15% based upon harmonic standard in IEEE standards 519-1992; 20% is assumed [2]. The maximum ripple can now be calculated from equation (2.6).DC link voltage, inductance, and the switching frequency decides the ripple current in this proposed system. The DC link voltage and

switching frequency are constant, thus the inductance can be calculated from equation (2.9):

$V_L = L\frac{\Delta\hat{I}L}{\hat{\delta}Ts}$, $\Delta\hat{I}L = \hat{\delta}T_S * V_L / L$ (2.5)

$\Delta\hat{I}L = \hat{\delta} * (V_L / L\ f_S)$

$= \frac{1}{6}(\hat{\delta}V_{DC} / Lf_S)$ (2.6)

$\hat{\delta} = 1 - \frac{1}{4} = \frac{3}{4}$ (2.7)

$\Delta\hat{I}L = \frac{1}{3}(V_{DC} / L\ f_S)$ (2.8)

$L = \frac{1}{8}(V_{DC} / \Delta\hat{I}L\ f_S)$ (2.9)

Where, V_L= Inductor voltage

f_S=Switching frequency

V_{DC} =DC link voltage

$\hat{\delta}$=Maximum duty cycle

At fundamental frequency, the reactive power supplied by the capacitor gives the capacitor C value. In this design reactive power can be chosen as 15% of the rated power is taken as reactive power which is given by (2.10)

$C = 15\%\ P_{rated} / 3 * 2\pi f * V^2_{rated}$ (2.10)

Table 1.Specifications Of LC Filter

V_{DC}	600V
I_{rated}	10A
P	6000W
F	50Hz
f_s	5000Hz
V	400V
ΔIL	1A

From the equation (2.9) and (2.10) the values of L and C are:

L= 15mH and C=4μf.

DESIGN OF PLL

PLL – Phase Locked Loop

PLL is commonly used in various sign packages e.g. radio- and telecommunications, computers and electric motor manage. The techniques can be adapted to work in a wide frequency spectrum from some hertz to orders of gigahertz. There are specifically three sorts of PLL systems for section monitoring: 0 crossing, stationary reference body and synchronous rotating reference frame (SRF) based PLL The SRF PLL is the one some of the above referred to with the first-class overall performance beneath distorted and non-perfect grid conditions [3] and is therefore the PLL system to be further investigated on this file.

THEORY

The basic concept of the PLL gadget is a feedback device with a PI-regulator tracking the phase angle. Input is the three phases of the grid voltage and output from the PLL is the section angle of one of the three levels. There could be one inverter leg for each of the 3 stages in energy deliver substation. There are two options, either assuming the grid voltages are in stability and tune only one of the stages after which shift with one hundred twenty levels for every of the alternative two stages or having three PLL systems, one for every segment.

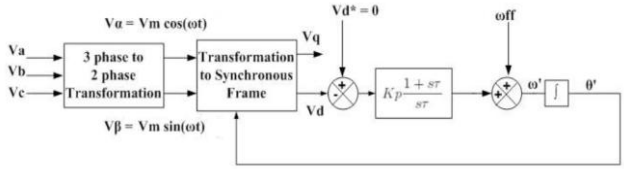

Fig3*Basic structure of SRF-PLL system*

Stationary reference frame $\alpha\beta$

To track the phase angle the three phase voltage signals V_a, V_b and V_c are transferred from three phases to a stationary system of two phases Vα and VβThe grid voltages are given as

$V_a = V_m \sin\theta$ (3.1)

$V_b = V_m \sin(\theta - \frac{2\pi}{3})$ (3.2)

$V_c = V_m \sin(\theta + \frac{2\pi}{3})$ (3.3)

where θ is the phase angle 2πft. The αβ-transformation matrix is given in equation (3.4)

$$T\alpha\beta = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2}\ \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}\sqrt{3}}{2}\ 2 \end{bmatrix} \quad (3.4)$$

Carrying out the matrix multiplication Vαβ = T$\alpha\beta$ V_{abc} yields

$$\begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} = \begin{bmatrix} Vm\sin(\theta) \\ Vm\cos(\theta) \end{bmatrix} \quad (3.5)$$

which is two signals carrying information only about the phase angle of one of the phases, Va.

Synchronous rotating reference frame

The phase angle is tracked by synchronizing the voltage space vector along q or d axis in the SRF [4]. Here the voltage space vector is synchronized with the q- axis see figure.4

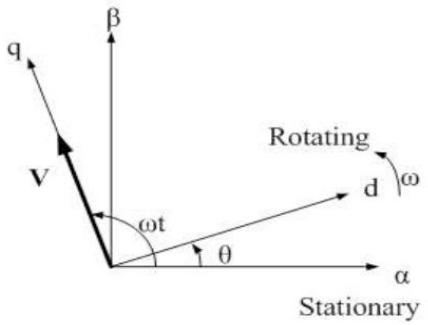

Fig4*Synchronous rotating reference frame*

If the voltage space vector is to be synchronized with the q-axis the transformation matrix is

$$T_{qd} = \begin{bmatrix} \sin\theta* & \cos\theta* \\ -\cos\theta* & \sin\theta* \end{bmatrix} \quad (3.6)$$

where θ* is the estimated phase angle output of the PLL system. Carrying out the transformation V_{qd} = $T_{qd}V\alpha\beta$ and using the trigonometric addition formulas yields (3.7).

$$\begin{bmatrix} Vq \\ Vd \end{bmatrix} = \begin{bmatrix} Vm\cos(\theta - \theta*) \\ -Vm\sin(\theta - \theta*) \end{bmatrix} (3.7)$$

The phase angle θ is estimated with θ* which is the integral of the estimated frequency ω'. The estimated frequency ω' is the sum of the PI-output and the feed forward frequency ωff. Gains of the PI-regulator is then designed so that Vd follows the reference value Vd * = 0, see figure 5.1. If Vd = 0 then the space voltage vector is synchronized along the q-axis and the estimated frequency ω' is locked on the system frequency ω. This results in an estimated phase angle θ* that equals the phase angle θ [3].

If θ* ≈ θ then the small angle approximation for sinus function yields V_d = -V_m(θ–θ*) and the structure in figure 3 can be simplified, see figure.5

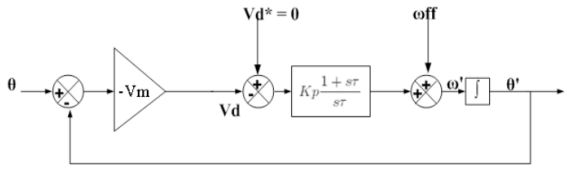

Fig5*Simplified system for the SRF-PLL*

The reason of the feed forward frequency, ωff, is to have the PI-regulator manipulate for an output sign that is going to zero. In our case the feed forward frequency may be 2πf = 100π. In the ideal case when the grid frequency is precisely 50Hz once the regulator has tracked the phase the output of the regulator is 0.

SIMULATION RESULTS:
OPEN LOOP SPWM INVERTER

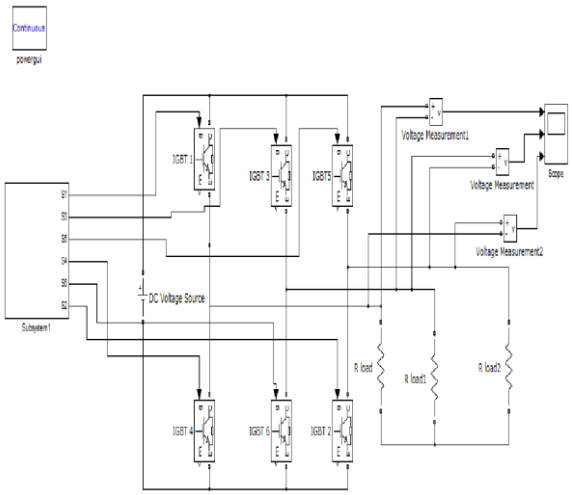

Fig6 *Simulation diagram of Open loop SPWM Inverter*

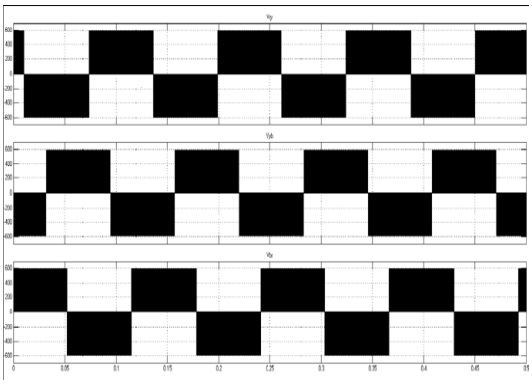

Fig7 *Simulation waveform of open loop SPWM inverter*

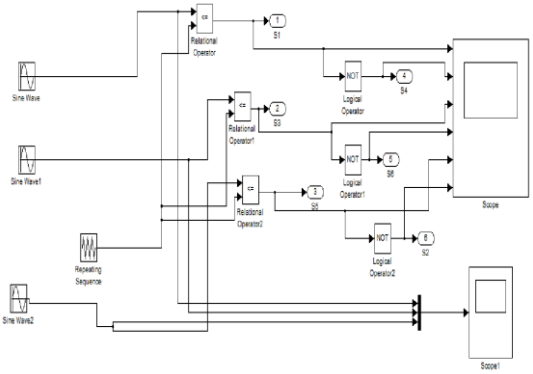

Fig8 *Simulation diagram of subsystem of 3 phase inverter*

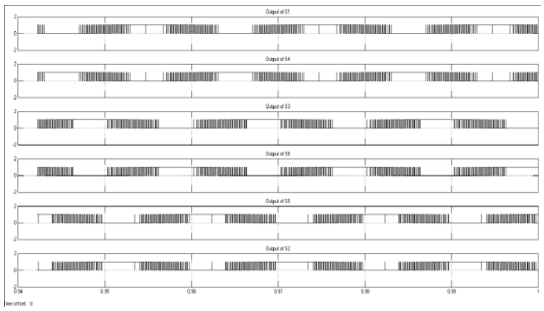

Fig9 *Simulation waveform of subsystem of 3 phase inverter*

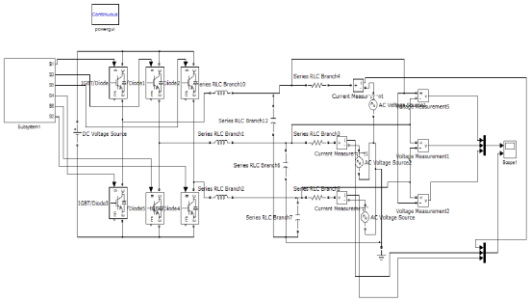

Fig10 *Simulation diagram of grid connected 3 phase inverter*

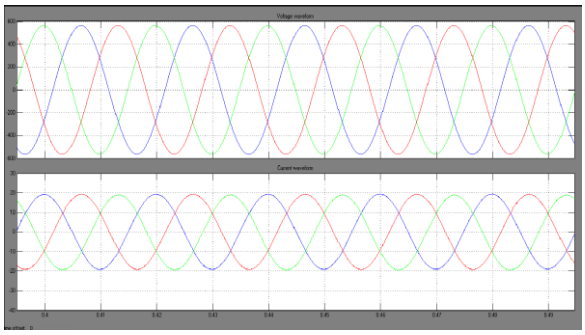

Fig11 *Simulation waveform of grid connected 3 phase inverter*

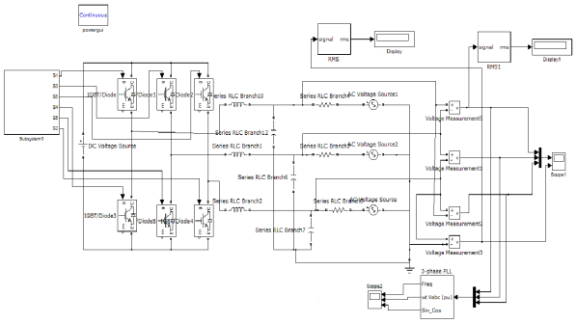

Fig12*Simulation diagram of frequency synchronization of grid by PLL*

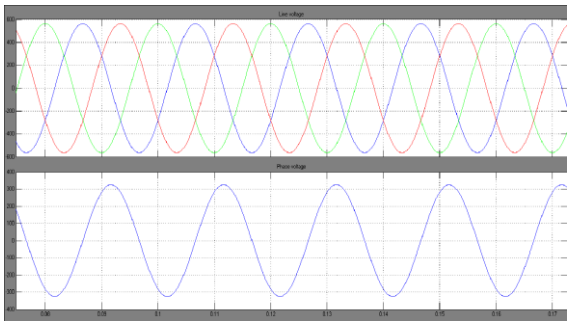

Fig13*Simulation waveform of frequency synchronization of grid by PLL*

SINE AND COSINE ANGLE OF PLL SYSTEM

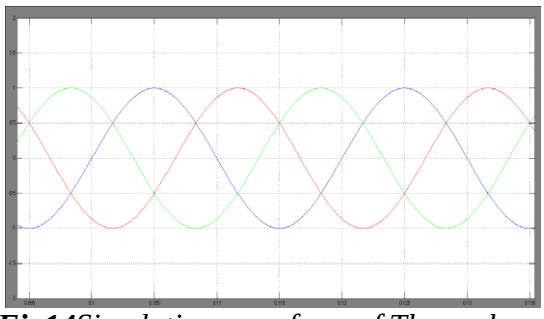

Fig14*Simulation waveform of Three phase voltage with* 120^0 *phase shift*

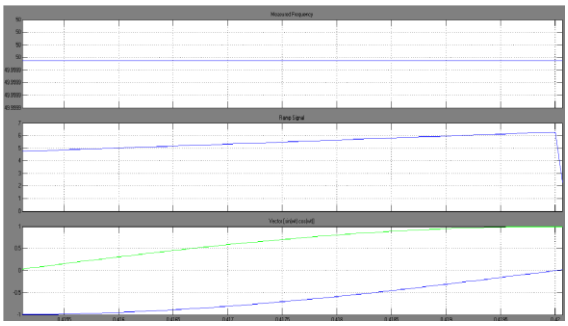

Fig15*Simulation waveform of Sine and Cosine angle after 90^0 phase shift*

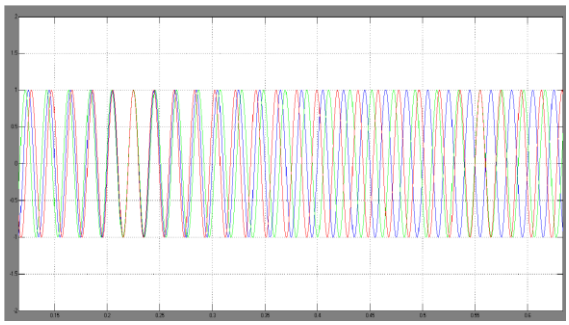

Fig16*Simulation waveform of unbalanced Three phase voltage*

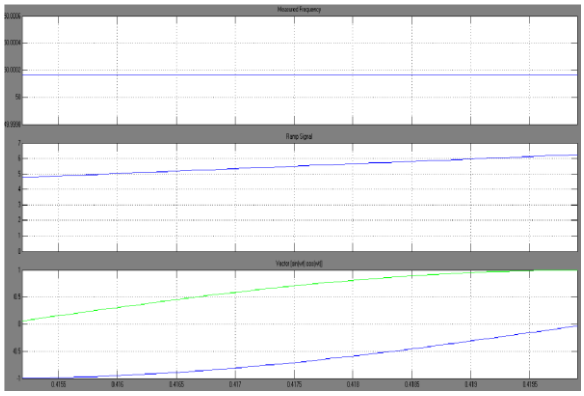

Fig17*Simulation waveform of Sine and Cosine angle after distortion*

CONCLUSION

Three phase inverter using sine PWM technique was simulated using MATLAB/SIMULINK. The values of filter inductance and capacitance were designed using the design specifications. The simulation of inverter tied grid connected system for grid synchronization using PLL technique was done. Program to generate variable duty cycle PWM was developed using Arduino IDE. Program to generate sine PWM was developed using Arduino IDE. The level shifter circuit to boost the Arduino output to 15V was designed and implemented. In near future, the hardware for PLL can be designed and connected to grid to synchronize the frequency of grid and to maintain it constant despite of varying loads.

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